REMARKS

Applicant no longer claims a small entity status for this application.

By the present Amendment claim 67 is cancelled. This leaves claims 20, 22-24, 27, 28, 33, 34, 36, 39-45, 47-50 and 65 pending in the application, with claim 20 being independent.

Claims 20, 22-23, 27-28, 34, 38-45 and 48 stand rejected under 35 USC 102(a) as being anticipated by Salatino et al (US 5,915,168). Claims 24, 33, 36, 47 and 49-50 stand rejected under 35 USC 103(a) as being unpatentable over Salatino and further in view of Ichikawa et al (US 5,996,199). Claim 65 stands rejected under 35 USC 103(a) as being unpatentable over Salatino and further in view of Chen (US 6,083,766).

Salatino describes a wafer level hermetically packaged integrated circuit. Ichikawa describes a method for manufacturing surface acoustic modules. Chen describes a packaging method of thin film passive components on silicon chip employing a ceramic or glass substrate mounted with the silicon chip so as to improve the mechanical strength of the components.

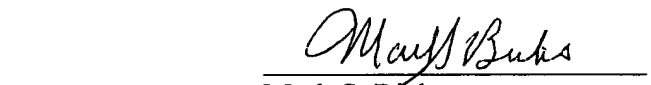
Applicant respectfully submits that none of the prior art, either alone or in combination, shows or suggests a method of producing a crystalline substrate based device including providing a wafer including a semiconductor substrate and comprising a plurality of semiconductor microstructures including at least one optoelectronic device, providing at least one wafer-level transparent packaging layer, forming onto said at least one wafer-level transparent packaging layer, a wafer-level spacer, said packaging layer and said spacer defining a plurality of cavities extending entirely through said spacer, sealing said wafer-

level spacer to said semiconductor substrate, thereby fully defining a gap between ones of said plurality of microstructures and corresponding chip scale portions of said at least one transparent packaging layer, without requiring removal of material from said at least one transparent packaging layer overlying said at least one optoelectronic device and subsequently dicing said semiconductor substrate, having said wafer-level spacer and said at least one wafer-level transparent packaging layer sealed thereunto, to form individual chip scale packaged devices, as recited in amended claim 20. Applicant respectfully submits that claim 20 is therefore deemed to be allowable.

Claims 22-24, 27-28, 33-34, 36, 39-42, 44-45, 47-50 and 65 depend directly or ultimately from claim 20 and recite additional patentable matter and are therefore deemed allowable.

In view of the foregoing remarks, all of the claims are believed to be in condition for allowance. Favorable reconsideration and allowance of the application is respectfully requested.

Respectfully submitted,



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